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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/761,790	01/21/2004	Albert E. Cosand	PD-03W012	3552

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EXAMINER	
NGUYEN, KHAI M	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 02/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/761,790	COSAND, ALBERT E.
	Examiner	Art Unit
	Khai M. Nguyen	2819

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 January 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *56-83* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *56-83* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *1/21/2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The indicated allowability of claims 56-83 is withdrawn in view of the newly discovered reference(s) (see below). Rejections based on the newly cited reference(s) follow.

Claim Objections

2. Claim 81 is objected because of the phrase, see line 1, "the first and sixth transistors" is not clear to the examiner. It should be read as "the fifth and sixth transistors". Correction or clarification is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 56-58, 60-81, and 82 are rejected under 35 U.S.C. 102(b) as being anticipated by Cake et al. (US 6,292,121).

Regarding claim 56, Cake et al. discloses (Figs. 5-6, 10-13) a delta-sigma modulator (see, the title) comprising:

a loop filter (315 of Fig. 11) (Cake uses the term "resonator" which acts or functions as a filter – see, column 9, lines 49-60);

a comparator (the comparator portion of the comparator & latch circuit 330 of Fig. 11 or 630 of Fig. 6) coupled to the loop filter (the resonator);

and a switch (350), wherein the switch comprising:

first means (i.e., the latch portion of circuit 330 or 630) for providing a first set of first and second complementary intermediate signals (output signals from circuit 330 or 630);

second means (the latch portion of circuit 340 or 640) for providing a second set of third and fourth complementary intermediate signals (output signals from circuit 340 or 640);

third means (differential transistor pair 652/654 of Fig. 6) responsive to the first set of signals for providing complementary output signals (at collectors of 652/654);

fourth means (differential transistor pair 656/658) responsive to the second set of signals for providing complementary output signals (at collectors of 652/654); and

fifth means (differential transistor pair 653/655) for selectively activating the third means or the fourth means in response to a control signal (from a source 620).

Regarding claims 57-58, Cake et al. discloses wherein the first means (of claim 1) corresponds to a master latch (i.e., the latch portion of circuit 330 or 630); and the second means corresponds to a slave latch (i.e., the latch portion of circuit 340 or 640).

Regarding claims 60-65, Cake et al. discloses the third means (of claim 56) including first and second transistors (the field effect transistors 652/654), which are connected in a common emitter configuration, (see Fig. 6), wherein the field effect transistors 652/654 are for formed by N-type and P-type semiconductor materials.

Regarding claim 66, Cake et al. discloses the invention of claim 61 wherein a first intermediate signal (first output of the first means) is provided as an input to the first

transistor (transistor 652 of Fig. 6) and a second intermediate signal (second output of the first means) is provided as an input to the second transistor (654 of Fig. 6).

Regarding claims 67-72, Cake et al. discloses the fourth means (of claim 61) including third and fourth transistors (the field effect transistors 656/658), which are connected in a common emitter configuration, (see Fig. 6), wherein the field effect transistors 656/658 are for formed by N-type and P-type semiconductor materials.

Regarding claim 73, Cake et al. discloses the invention of claim 68 wherein a third intermediate signal (first output of the second means) is provided as an input to the third transistor (transistor 656 of Fig. 6) and a fourth intermediate signal (second output of the second means) is provided as an input to the fourth transistor (658 of Fig. 6).

Regarding claims 74-79, Cake et al. discloses the invention of claim 67 wherein the fifth means (differential field effect transistor pair 653/655) includes a fifth transistor (653) and a sixth transistor (655) which are connected in a common emitter configuration (Fig. 6), wherein the field effect transistors 653/655 are for formed by N-type and P-type semiconductor materials.

Regarding claim 80, Cake et al. discloses the invention of claim 75 wherein inputs to the fifth and sixth transistors are provided by complementary clock signals (column 7, lines 24-33).

Regarding claims 81-82, Cake et al. discloses the invention of claim 80 wherein the fifth (first) and sixth transistors (653/655) have a terminal connected to a current source (650) and a terminal connected to one of the first differential pair (652/654) and the second differential pair (656/658).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 59 is rejected under 35 U.S.C. 103(a) as being unpatentable over Cake et al. (US 6,292,121) in view of Cheng (US 6,396,428). Cake et al. discloses the delta-sigma modulator of the claimed invention (of claims 56-58) except for the first and second latches are coupled in series as claimed. Cheng discloses (Fig. 1) a delta-sigma modulator (see the title & abstract) comprising a resonator 10 (column 3, lines 4-12), a clocked comparator (11A), a first or master latch (11B), and a second or slave latch (11C) serially connected to the first latch (column 3, lines 39-41). Thus, it would have been obvious to one person having ordinary skills in the art at the time the invention was made to modify the connection of the latches (of circuits 330/630 and 340/640) as suggested by Cheng (see Fig. 1) for improving the noise shaping of the delta-sigma modulator (column 3, lines 20-25).

Claim 83 is rejected under 35 U.S.C. 103(a) as being unpatentable over Cake et al. (US 6,292,121) in view of Watson (US 6,445,322). Cake et al. discloses the claimed invention (82) except for the current source is a cascode current source. Watson discloses an apparatus (see Fig. 1B or 2) wherein a DAC current switch or steering cell (transistor pair 102a/b or 204/205 which is equivalent to the means) is coupled to a cascode current source (103/151 or 210). Therefore, it would have been obvious to one

person having ordinary skills in the art at the time the invention was made to use a cascode current source as suggested by Watson for providing a current to the fifth means (of claim 56) because the cascode current source has high output impedance, therefore, a high noise immunity is achieved with respect to noise in the output terminal of the current source (column 1, lines 33-41).

Contact Information

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khai M. Nguyen whose telephone number is 571-272-1809. The examiner can normally be reached on 9:00 - 5:30 Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rexford (Rex) Barnie can be reached on 571-272-7492. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Khai M. Nguyen
Art Unit: 2819

571-272-1809

REXFORD BARNIE
SUPERVISORY PATENT EXAMINER